

A Comparative Study On Low Power Adders For Wearable Devices

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Abstract: An adder is a device used to perform arithmetical functions in electronic calculators and digital instruments and has a wide range of applications. The major factor involved in driving all these instruments is Power. As the power consumption of a device increases, the life span of device reduces. In order to maintain longer life of the device, it is necessary that the power consumption is less. A device is considered efficient when it consumes low power and has high speed. The purpose of this study is to investigate the power and delay product of the adders. The adders that have been compared are all of 12 bit and have been synthesized and simulated using the Cadence software. The outcomes of different properties obtained from the synthesis reports and simulation of the circuit helps in finding out the adder with minimum power and delay product. The adders that have been compared in this paper are Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA), Carry Increment Adder (CIA), Carry Select Adder (CSA) and Kogge Stone Adder (KSA).

Index Terms Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA), Carry Increment Adder (CIA), Carry Select Adder (CSA), Kogge Stone Adder (KSA), Low Power, Wearable devices.

1 INTRODUCTION

Ever since its inception, technology has been changing the world. While the advancements in technology have influenced people in all walks of life, the need for a commendable system efficiency has always demanded for improved performance characteristics. Adders are among the majorly used components in processing units and find a wide range of applications, that include, microcontrollers, arithmetic logic circuits, timers, etc.[1] They are the key components in almost all the digital processing units. Extending their use beyond vast and complex circuitries, adders in the recent past have gained a huge prominence in several portable devices as well. Amongst the various features of portable devices, reduced power dissipation coupled with quicker operability and device compactness form the all time primary requirement.[2] Adders being a crucial part of such devices, are therefore the most favorable target units that have left a room for improvement, thus accelerating and encouraging detailed research in this domain. Binary adders perform binary addition on the given binary inputs. Of all the existing adders, the single-bit adders, viz. Half adder and Full adder circuits form the leaf cells to various other multi-bit adder circuits. The full adder varies from a half adder, in that, in addition to the 2 input binary bits, it also takes an input carry bit and performs addition. The general expression for Sum and Cout of a half adder with 2 binary bits A and B can be given as,

$$\begin{aligned} \text{Sum} &= A \oplus B & 1 \\ \text{C}_{out} &= AB & 2 \end{aligned}$$

On similar lines, the expressions for Sum and Cout of a single-bit Full adder with three inputs, including A, B and the input carry Cin can be given as,

$$\begin{aligned} \text{Sum} &= A \oplus B \oplus C_{in} & 3 \\ \text{C}_{out} &= AB + AC_{in} + BC_{in} & 4 \end{aligned}$$

Moreover, it should also be noted that a single-bit full adder can be built using two separate half adders and an OR gate. The Half adder and Full adder forms the basis of all other adders in the digital domain.[3] A multi-bit adder takes inputs of length greater than 1 bit. A number of such Half adders and Full adders are cascaded in different manner to provide varied performance characteristics in multi-bit adders. This paper presents a comparative study on the various

multi-bit binary adders, by evaluating their key features such as power, delay, area, etc. The next section gives a detail on the operation of five types of existing multi-bit adder circuits, including the Ripple Carry adder, Carry Look Ahead adder, Carry Increment adder, Carry Select adder and the Kogge Stone adder, along with their power delay product and area computed using Cadence NC Launch simulator. The results obtained will then be compared in the sections to follow, with a prime objective of identifying the best performing adder with regard to power, delay and area for applications in various existing and emerging fields.

2 EXISTING MULTI-BIT BINARY ADDER CIRCUITS

2.1 Ripple Carry Adder

Ripple carry adder (RCA) accepts two binary numbers to be added, along with the carry input.[4] The circuitry is quite simple and comprises full bit adders connected in series. Each of the full adders in the ripple carry adder circuit has three inputs and two outputs. While two of the inputs are the two numbers to be added, the third input is the carry that is obtained from the previous stage. While Cin is the initial carry input, the carry out obtained at the output of each full adder, forms the carry input for the next full adder. The design follows a bottom-up approach, where 'n' number of leaf cells such as half adders and full adders are finally combined to get the n-bit ripple carry adder.[5](see Fig 1.)

2.2 Carry Look Ahead Adder

Carry Look Ahead Adder is an adder circuit with greater speed than the Ripple Carry Adder (RCA) [6]. It boosts the speed by computing one or more carry bits before the sum thus, reducing the propagation delay. The concept of generate and propagate carries is used in this adder logic.(see Fig. 2) The propagate carry (Pi) and the generate carry (Gi) is found using the following equations.[7]

$$\begin{aligned} P_i &= A_i \oplus B_i & 5 \\ G_i &= A_i B_i & 6 \end{aligned}$$

A 12-bit sum (Si) and carry output (Ci) is computed as:

$$\begin{aligned} S_i &= P_i \oplus C_i & 7 \\ C_{i+1} &= G_i + P_i C_i & 8 \end{aligned}$$

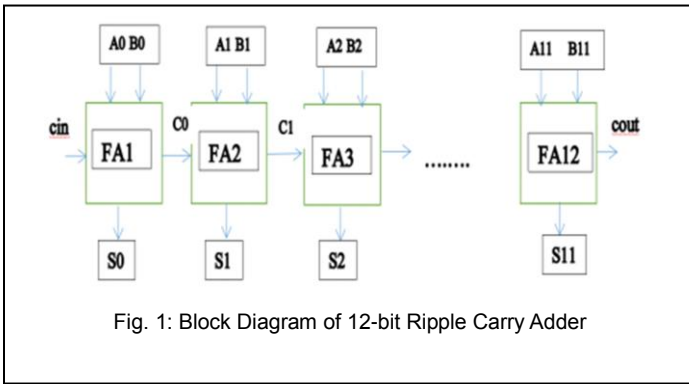


Fig. 1: Block Diagram of 12-bit Ripple Carry Adder

operation performed on the carry out of the second CLA and the carry out of the last half adder.[8] (see Fig. 3).

2.4 Carry Select Adder

A n-bit carry select adder (CSA) consists of two n-bit ripple carry adders and a multiplexer. Since, two ripple carry adders are used, addition of the numbers is done twice. The input carry value of one of the ripple carry adders is logic 1 and the input to the other ripple carry adder is logic 0. Once the computation is done, the appropriate sum and carry-out is determined with the help of the multiplexer. The computational speed in carry select adder is greater compared to the other adders. However, the complexity in the circuit, higher power consumption and larger area utilization serves as a drawback.[9](see Fig. 4)

2.5 Kogge Stone Adder

Kogge-Stone Adder (KSA) is a type of Parallel Prefix adder containing Propagate and Generate bits. The KSA has three major computational stages, viz. The pre-processing stage, the carry generation stage and the post processing stage.[10](see Fig. 5.)

2.5.1 Pre Processing Stage

This stage consists of obtaining the propagate and generate terms corresponding to the two 12-bit inputs (A and B) given. The logical expression to obtain the propagate and generate terms are as follows:

$$\begin{aligned} \text{Propagate: } P_i &= A_i \oplus B_i & 9 \\ \text{Generate: } G_i &= A_i B_i & 10 \end{aligned}$$

2.3 Carry Increment Adder

The Carry Increment Adder circuit contains Carry Look Ahead

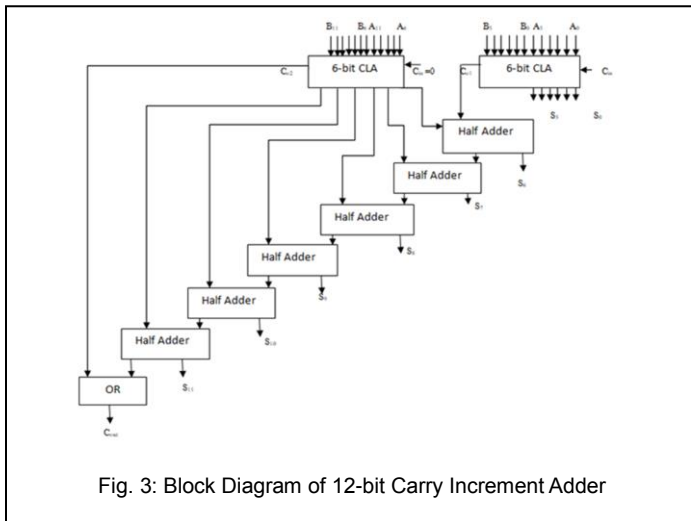


Fig. 3: Block Diagram of 12-bit Carry Increment Adder

Adder and the incremental circuitry which is made up of half adders. A 12-bit adder can be designed by using two 6-bit CLA. The first CLA adds the first 6-bits of the input to produce a 6-bit partial sum and a carry. Therefore, the first 6 bits of the final sum is obtained from the first CLA. The remaining 6 bits of the input are given as inputs to the second CLA with a fixed input carry value of zero. The partial sum obtained from this second CLA is given as the input to the incremental circuit which has six half adders. The input to the half adders is the partial sum of second CLA and the carry out of the previous adders. The final carry out of the circuit is the output of OR

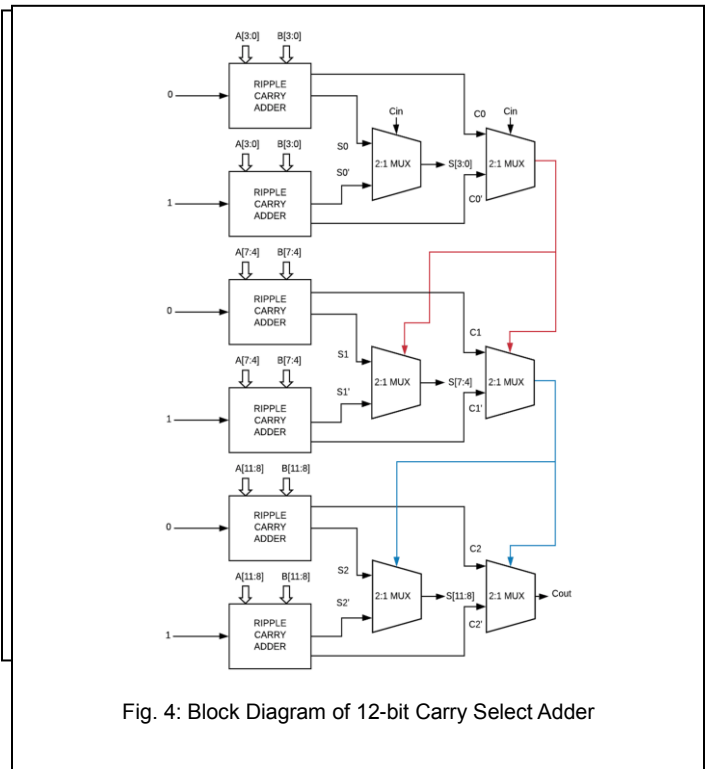


Fig. 4: Block Diagram of 12-bit Carry Select Adder

2.5.2 Carry Generation Stage

This stage consists of the involvement of the carry signals through a group of propagate and generate bits. There are a number of vertical stages of computation to be performed

based on the number of bits in the input. For a 12-bit Kogge-Stone adder, there are four stages of intermediate propagate and generate terms. The logical expressions are as follows:

$$\begin{aligned} \text{Intermediate Propagate } P_{i:j} &= P_{i:k+1}P_{k:j} & 11 \\ \text{Intermediate Generate } G_{i:j} &= G_{i:k+1} + (P_{i:k+1}G_{k:j}) & 12 \\ \text{Intermediate Carry } C_i &= G_i & 13 \end{aligned}$$

2.5.3 Post Processing Stage

This is the final stage of the Kogge-Stone adder circuit used to obtain the sum and carry outputs of the adder. The logical expression to obtain the sum is:

$$\text{Sum: } S_i = P_i \oplus C_{i-1} \quad 14$$

Where C_{i-1} is the intermediate carry generated in the carry look-ahead network stage

3 RESULTS AND COMPARISON

In recent times, as the number of wearable devices is increasing rapidly, and the size of mobile devices is decreasing, circuits consuming minimum power, occupying less area and having a minimal delay are required. The five types of adders mentioned in this paper were implemented in Verilog using Cadence (NC Launch) tool, with 45nm technology (FreePDK45 Library). The number of cells, area in μm^2 , power in nW and timing in ps were obtained

TABLE 1
COMPARISON OF ADDERS

Comparison of Adders					
Adder	No of Cells	Area (μm^2)	Power (nW)	Delay (ps)	PDP (fWs)
Ripple Carry Adder	60	83	2689.104	7212	19.3938
Carry Lookahead Adder	63	78	2198.836	4046	8.8964
Carry Increment Adder	64	85	2571.477	3857	9.9181
Carry Select Adder	150	184	5479.84	3258	17.8533
Kogge Stone Adder	48	57	1971.837	4509	8.8310

The power delay product (also known as switching energy or PDP) which is a figure of merit correlated with the energy efficiency of the logic gates, is used as the basis for the analysis. The PDP obtained here is expressed in femto watt-seconds (fWs). Table 1 contains the parameters mentioned above and the power-delay products of the five adders. Graphical representations of adder comparisons based on their power, delay and PDP using bar charts are also provided. Ripple Carry Adders, though simple to implement, consume a substantial amount of power and delay. Carry Look Ahead Adders and Carry Increment Adders consume lesser power and are faster when compared to Ripple Carry Adders. Carry Select Adders are known for their ability to compute with high speed. Unfortunately, they are power-hungry due to their complex circuitry. Whereas Kogge Stone Adders are both fast and power-efficient, as a result, have the least power-delay product when compared to the

other adders mentioned before. The cell count and the area occupied is also less, and thus, it is favourable to use in mobile computing devices and IoT applications.

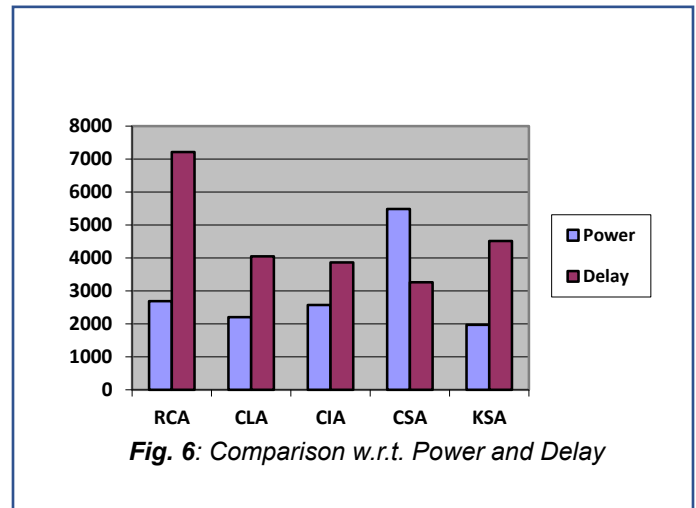


Fig. 6: Comparison w.r.t. Power and Delay

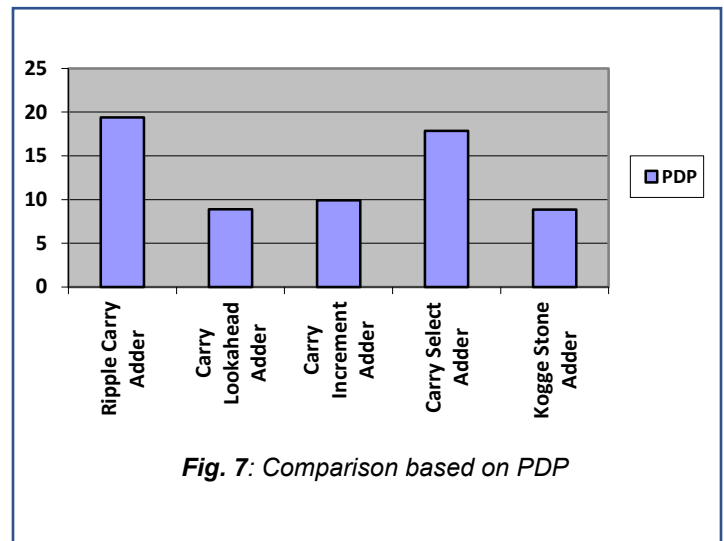


Fig. 7: Comparison based on PDP

4 CONCLUSION

In this paper, five different types of adders were compared viz; Ripple Carry Adder(RCA), Carry Look Ahead Adder(CLA), Carry Increment Adder(CIA), Carry Select Adder(CSA) and Kogge Stone Adder(KSA). Various parameters such as number of cells, area, power, delay and power delay product were obtained. The comparison of these adders was mainly based on the power-delay product since it would highlight the fastest and the most power efficient adder out of the adders chosen in this paper. The least power delay product was observed in case of the Kogge Stone Adder (KSA) which also occupied the least area. All these factors make KSA favourable in IoT applications and mobile computing devices.

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