A Robust, High Performance And Low Power (HPLP) 8T SRAM Cell For Iot Applications

Sargunam TG, C.M.R.Prabhu, Lim Way Soong

Abstract: The significant development of memories with embedded on-board SRAM has been increasing tremendously for the current Internet-of-Things (IoT) applications. The high performance and low power SRAM cells are critically important and play a vital role for the data computations in any IoT application. The SRAM Cells are generally important for the contemporary VLSI systems and applications. The on-board SRAM memory demand is increasing day by day with the additional requirements of less power consumption, improved stability, improved performance, and overall energy efficiency. This research work presents a High Performance and Low Power (HPLP) SRAM cell with 8 transistors. The presented cell is designed in CMOS technology and simulation was carried out using Cadence Virtuoso EDA tool. The suggested HPLP SRAM cell's write power analysis confirms that 47% write power is reduced. The write ability has been improved and the write delay has also been improved by 24% for write operations. Furthermore, the HPLP cell is robust and stable in worse environmental conditions with range of temperature from -50^{o}C to 150^{o}C.

Index Terms: SRAM Cell, Low Power, High Performance, Delay, Stability, Robust, IoT,

1. INTRODUCTION

There is a tremendous growth in Wireless Sensor Network and Internet of Things (IoT) applications with its multiple number of easily connected and battery-operated devices. All IoT applications are persistently demand the battery devices' operating lifetime to be extended. The consistent and faster memories are always required to store and compute the data for any present IoT application and for any modern portal gadgets. The use of mobile appliances, personal digital assistants, smart phones, and portable gadgets are becoming part of the daily life. In particular, the smart phones and mobile devices have predominantly become main part of everybody's life. The mobile gadgets are produced with continuous developments to cover many applications and taking different dimensions of features and specification. This rapid improvements in mobile devices extremely demand product success and sustainability [1]. Large amount of data is being processed by such devices especially on media data for live streaming. There is continuous increase and high demand for fixed memory in terms of its usage for processing multimedia applications. The power consumption and limited operating lifetime of battery can be affected in these applications. Summarising all the above, the demand for an extended battery lifetime is essential and has been increasing. Further, this can avoid the human efforts to frequently replace the batteries and at times it is too challenging to power-up these IoT devices due to their remote deployment and smallest size factor etc.

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Therefore, the low power consumption and higher performance have become main constraints for the up-to-date IoT based system-on-chip (SoC) in digital VLSI system designs. To meet this ever-increasing requirement of on-chip computational processing in IoT applications, the SRAM is always ideal due to its unique characteristics: high performance, rapid response, and low power consumption. It is confirmed from the literature that power consumption of SRAM is always high compared to the overall power of the system. About 40% to 50% of dynamic energy is being constantly consumed by SRAMs memory in high performance SoCs. The on-chip SRAM cache normally consumes a major portion of overall total power per operation. SRAM is critical and one of the repetitive architectures in VLSI systems. There are so many budding cells developed by researchers with characteristics such as high speed, increased stability, low power, and overall performance. These characteristics of SRAM cells are becoming mandatory requirement to meet the continuous industry requirements on various modern VLSI development [2,3]. The VLSI performance is generally improved by SRAM cells as they play a vital role [4-7]. The power and supply voltage are though equivalently decreased, the performance in terms of speed and stability are degrading. The many earlier proposed cells' Static Noise Margin (SNM) and overall performance [8-11] are to be improved. Generally, there were various write and read assist methods have been proposed and designed to overcome the power and stability issues. Some of the common ones are power gating with different supply voltage, single bit-line operation, Schmitt trigger design, staff effect and separate read circuit. The SRAM cell's read stability is normally improved by having a separate read circuit which isolates the storage nodes from the read path. There were many SRAM cells proposed earlier using CMOS and FinFET technologies and deployed with different techniques. Despite of having all these common improving factors, it is observed that the conventional SRAM cells are not highly suitable for Internet of Things (IoT) based low power applications [13]. Considering the above requirements for SRAM cell development in terms of low power, high performance, improved read stability and write ability, this research work presents the High Performance and Low Power (HPLP) SRAM cell with below significant features:

- To improve write power, performance and stability, the suggested cell is constructed with additional 2 signals namely (LW & RW).
- The discharging activity is less at the bit-lines causes less power consumption during the write operations.
- The voltage and temperature variations are applied to measure the power and delay.

The remainder of this research paper is organized as follows: Section 2 presents the architecture and describes the operation of the suggested High Performance and Low Power cell. Section 3 discusses and compares the conventional cells with simulation results. The concluding remarks are presented in Section 4.

2. ARCHITECTURE OF HPLP CELL

The suggested HPLP cell is designed to minimize the power without having any trade-off between delay and stability. The cell's schematic diagram is shown in Figure.1. There are 8 transistors used to design this HPLP cell in 180nm CMOS technology. This novel cell has two inverters in the name of InverterL and InverterR. The InverterL is connected by the M1 and M2 transistors The M3 and M4 transistors form the InverterR. During the write operations, transistors M7 and M8 performs an important role and these two transistors are connected to two different signals namely LW and RW. These two signals control the transistor M7 and M8 functions alternatively. The BL and nBL bit-lines are connected with respective output nodes Q and NQ through the transistors M5 and M6. These two transistors M5 and M6 do function as the access transistors. The WL (word-line) and LW and RW signals perform the write operations in this HPLP cell. The signals LW and RW are kept ON alternatively and thus the respective data is transferred faster at the output nodes Q and NQ.

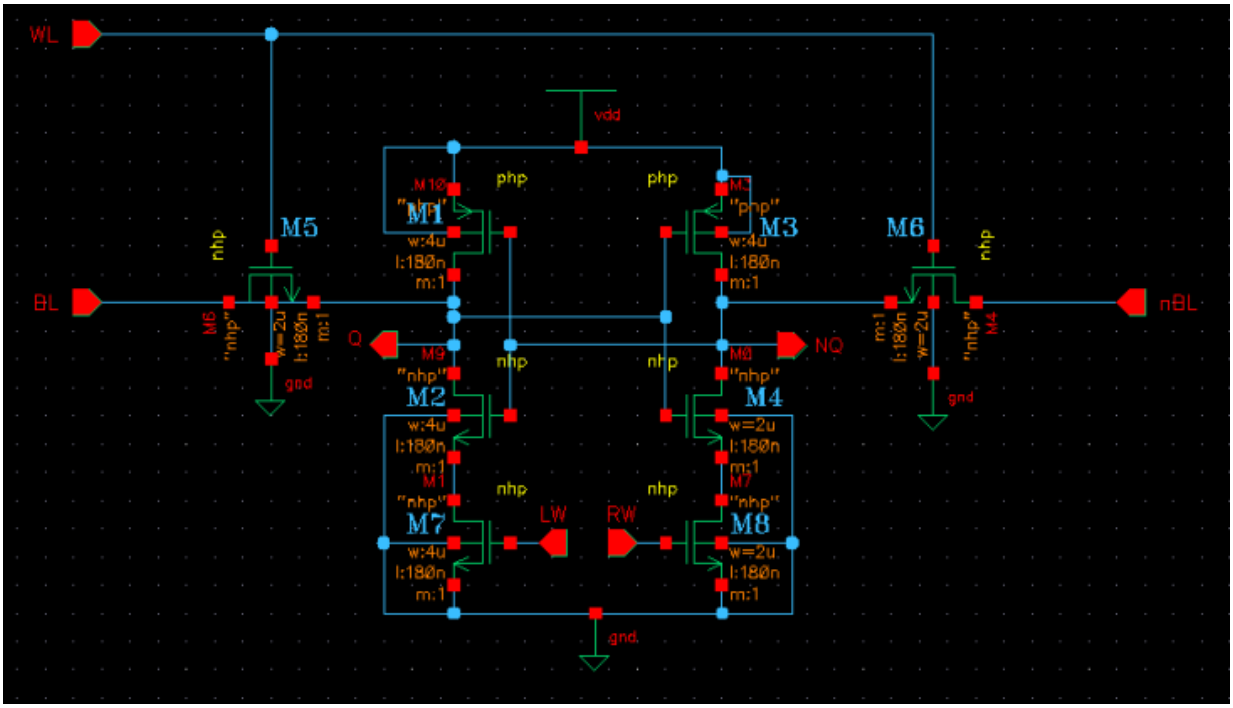


***Fig.**1 HPLP SRAM Cell Schematic Diagram*

2.1 Write Operation

The dynamic nature of HPLP cell switches the data easily at the output nodes through M5 and M6 access transistors. Once the data to be written are assigned at BL and nBL (bit-lines) and WL (word-line) is asserted to be high. The write ability is improved by the signals LW and RW which performs a major role in this circuit instead of the word-line WL.

a. Write '1' Operation

In this proposed HPLP cell, the write '1' operation is performed by setting the bit-line BL to '1' and nBL to '0'. The word-line WL is asserted to high. Before the word-line is asserted, the signal LW is set to '0' and signal RW to '1'. This makes the tail transistors M7 is disconnected from the ground and M8 is connected to the ground which causes the data to be written in output node Q. When the bit-line nBL is set to '0' and the signal LW is again to set to '0'. Hence the tail transistor M7 is turned off which makes the InverterL's pulldown path is disconnected. This flips the node Q to '1' without waiting for nBL to fully discharge.

b. Write '0'Operation

For the write '0' operation, the nBL is set to '1' and then the word-line WL is set to high. The signals LW and RW are set to '1' and '0' respectively much before asserting the word-line. Thus, the M7 tail transistor is connected and M8 is disconnected from ground terminal which triggers the data '0' to be written in NQ output node. On the other hand, when BL is set to '0', the M8 tail transistor turned to be off

because the RW signal is also set to '0' and hence disconnects the pulldown path of InverterR. This instantly flips the output node NQ to '1' without a wait for BL bit-line to completely discharge. The write power consumption has been minimized and write delay has been improved due to the impact on disconnection of pulldown path of the inverters. The RW and LW signals are set to '1' when read operation takes places and during the hold mode.

2.2 Read Operation

Both bit-lines BL and nBL are pre-charged during the read operation. The read operation is carried out by the transistors M5, M2 and M7 and M6, M4 and M8 for read '0' and read '1' respectively when the WL is asserted to high. In the read '0' operation, the output at Q (Q=0) is discharged through the transistors M5, M2 and M7. In the read '1' operation, the stored output at Q (Q=1) is discharged through the transistors M6, M4 and M8.

3. SIMULATION RESULTS AND DISCUSSION

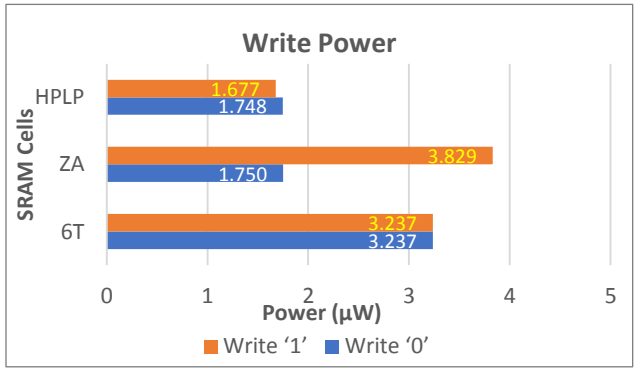
This part of the paper presents the simulation results of the proposed HPLP cell and conventional 6T and Zero Aware SRAM cells. The write power and write delay at variation of V_{DD} and temperature are compared, and the results are presented.

3.1 Simulation Setup

As per the International Technology Roadmap for Semiconductors (ITRS) normally determines the short-term and long-term objectives and key technical requirements of the semiconductor and related industrial applications [14]. The HPLP cell and conventional cells have been designed and deployed in a standard 180nm CMOS technology. The simulations were also carried out in similar technological environment. The performance, power, delay on PVT variations of HPLP cell have been compared with conventional cells. There are strategic similarities between the proposed HPLP and conventional cells. A uniform device sizing and 1.8V are maintained for the simulation in Cadence Virtuoso environment for a fair comparison [15]. The simulation results of HPLP cell are analysed in terms of power, delay, variation of write power consumption and delay at various V_{DD} ranges from 1.8V to 0.8V are presented in this section. Further, the variation of power and delay with temperature range from -50^{o}C to 150^{o}C are also presented.

3.2 Write Power and Write Delay

The discharging happens at two bit-lines in the conventional 6T SRAM cell due to which it consumes more power. Alternatively, the power for write '0' operation in ZA SRAM cell is less due to one bit-line [4] and single tail transistorWhereas, in the proposed HPLP cell, the tail transistor M7 or M8 disconnects the pull-down path during the write operations. This causes the write power and write delay to minimize as shown in the Fig.2 and Fig.3.



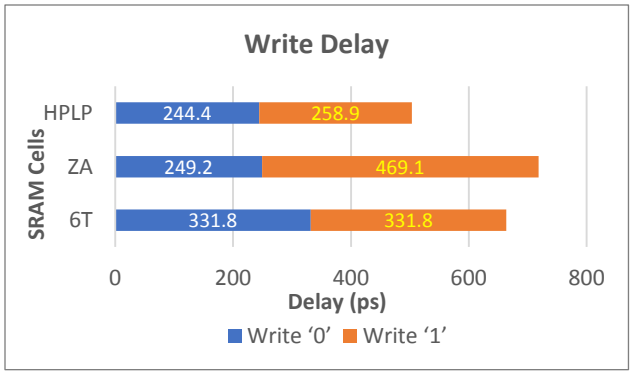


***Fig.3** Write delay*

The write '0' power of the suggested HPLP cell is 46% less when compared to conventional 6T cell. On the write '1' operations, 48% is less against 6T cell. The write access time is also been improved about 26% for write '0' and 22% for write '1' operations against 6T SRAM Cell. When compared to ZA cell, the write access time is improved to 54% and 45% for write '0' and write '1' operations, respectively. Overall, there is an average of 47% write power and 24% write delay have been improved against conventional 6T cell. The proposed HPLP cell, 6T SRAM and Zero Aware cells have been simulated with varying supply voltage V_{DD} from 1.8V to 0.8V to understand and cell operation and stability [15]. The average write power and write delay has been compared with the 6T SRAM cell. For the write '0' operation, the proposed HPLP cell confirms that it works even at 0.8V. There is an average of 45% power is less comparing with 6T when the range of voltage (1.8V – 0.8V) is applied for write '0' operations. The write access time is also improved by 13% against 6T cell for write '0' operation. The write '0' power consumption and the respective delay are presented in Fig.4 and Table.1.

Table.1 Write delay on various V_{DD}

V_{DD} (V)	Write '0' Delay (ps)		
	6T	ZA	HPLP
1.8	331.8	249.2	244.4
1.7	339.8	261.7	260.3
1.6	346.8	278.5	276.8
1.5	358.9	296.1	293.4
1.4	369.7	317.6	311.9
1.3	384.2	333.8	332.3
1.2	401.7	357.9	354.2
1.1	421.6	387.0	382.3
1.0	444.9	421.4	416.3
0.9	-	465.1	457.9
0.8	-	515.8	510.3

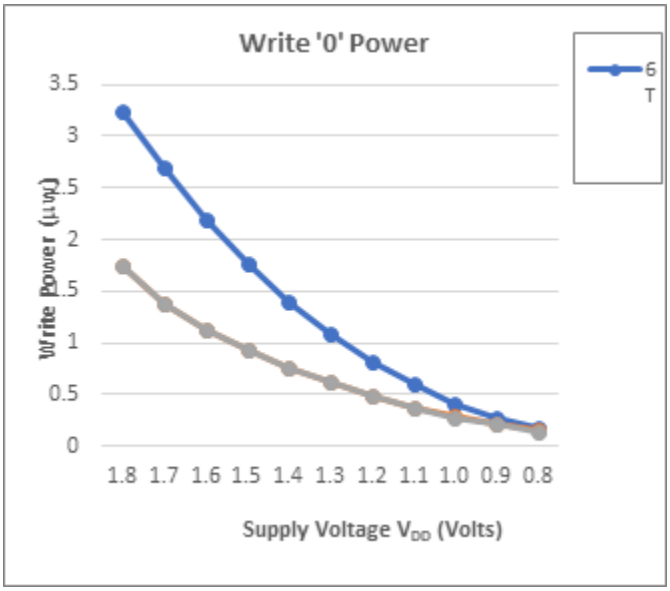


***Fig.**4 Variation of write '0' power on various V_{DD}*

The proposed HPLP cell, 6T SRAM and Zero Aware cells have been simulated with varying supply voltage V_{DD} from 1.8V to 0.8V to understand and cell operation and stability for write '1' operation as well. The average write power and write delay has been compared with the 6T and ZA SRAM cells. For the write '1' operation, the proposed HPLP cell confirms that it can work even at 0.8V whereas the 6T and ZA cells can last only up to 1.0V. An average of 44% and 57% power is less compared with 6T and ZA cells when the varying voltage (1.8V – 0.8V) is applied for write '1' operations. The write access time is also improved about 13% against 6T cell and 37% respectively. The write '1' power consumption and the respective delay are presented in Fig.5 and Table.2 as shown below:

Table.2 *Write delay on various V_{DD}*

V_{DD} (V)	Write '1' Delay (ps)		
	6T	ZA	HPLP
1.8	331.8	469.1	258.9
1.7	339.8	473.4	271.6
1.6	346.8	479.6	286.0
1.5	358.9	483.5	302.8
1.4	369.7	495.9	318.8
1.3	384.2	505.5	338.4
1.2	401.7	525.2	362.2
1.1	421.6	560.0	390.3
1.0	444.9	627.8	423.2
0.9	-	-	464.3
0.8	-	-	515.9

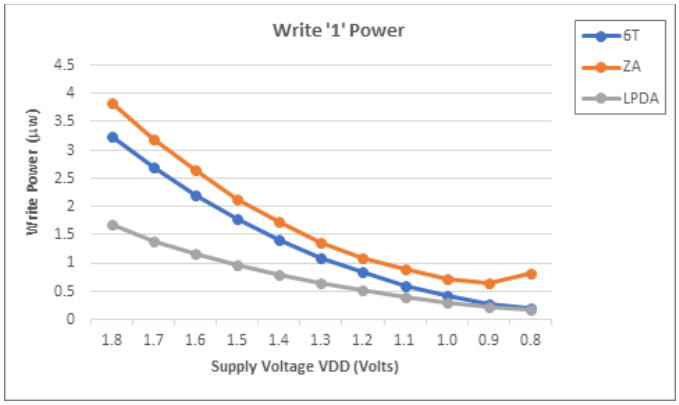


Fig.5 *Variation of write '1' power on various V_{DD}*

The proposed HPLP cell has been simulated and tested for the write power with a range of temperature from -50°C to 150°C against 6T SRAM cell. There is an average write power of 45% is reduced compared with the cell. The suggested HPLP cell is also been tested for its stability with temperature range from -50°C to 150°C against conventional 6T SRAM cell [16]. An average delay of 33% has been improved when compared with 6T cell. The simulated results with various temperatures on the write power and write delay are shown in Fig.6 and Fig.7 as below. The simulated results prove that the HPLP SRAM cell can be applied in any worse condition (T=150°C) with minimum power loss.

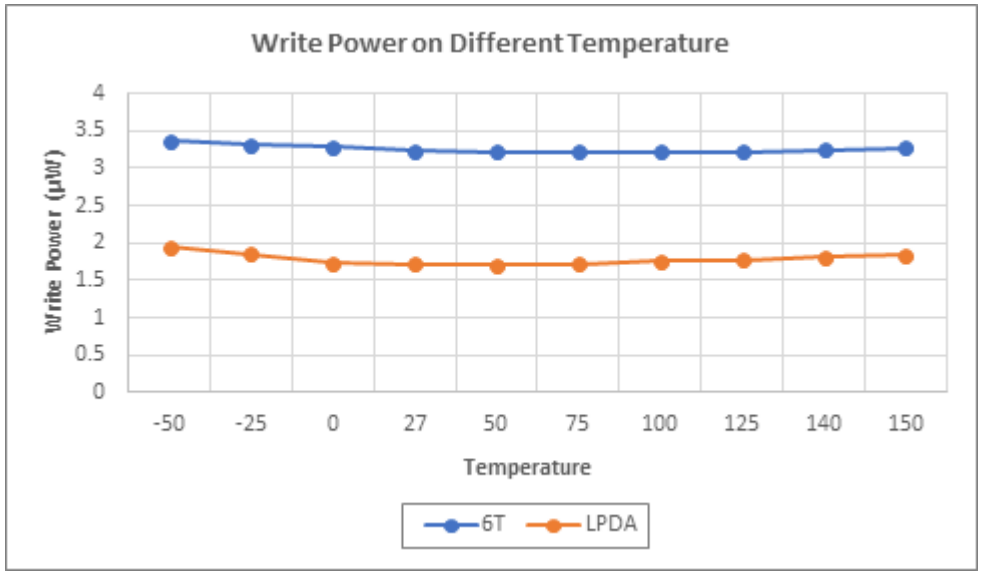


Fig.6 *Variation of write power on different temperature*

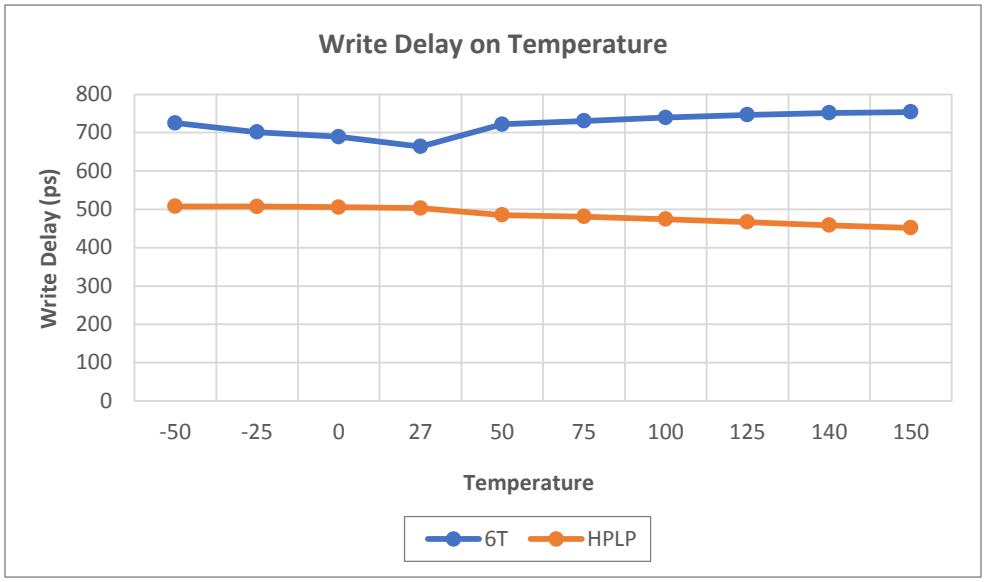


Fig.7 *Variation of write delay on different temperature*

3.3 Read Power and Read Delay

For the read operation, the proposed cell's read power is higher than the 6T cell and almost similar to the ZA cells for both read '0' and read '1' operations [17]. The read delay is also more when compared to the conventional cells. There is no power reduction or any improvement of read access time during the read operations. Moreover, the read operations are performed by the transistors in the circuit without a separate read circuit. The read delay and read power are shown in Fig .8 and Fig.9.

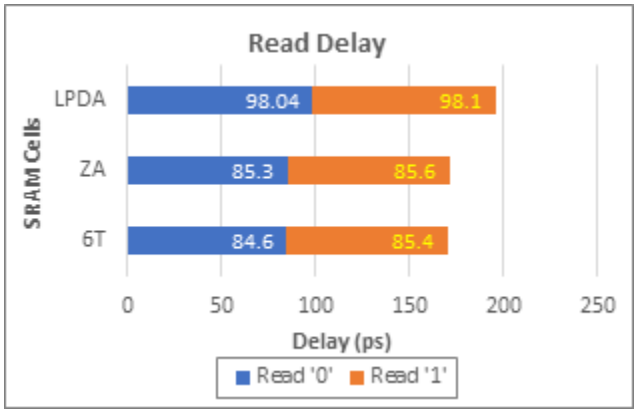


Fig.8 Read delay

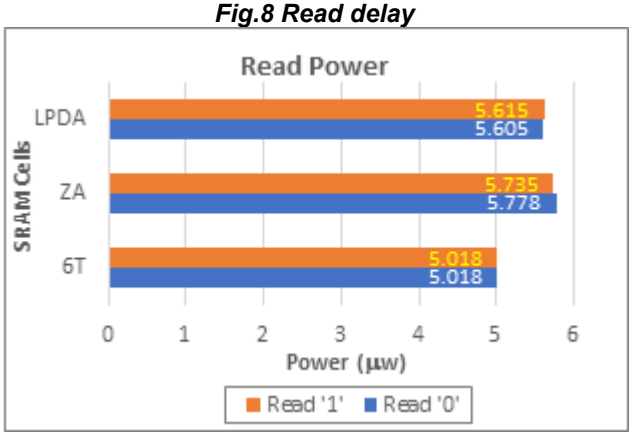


***Fig.9** Read power*

4. CONCLUSION

It is concluded that many such techniques with less power consumption has been deployed to reduce the power during the write operation. The suggested HPLP SRAM cell reduces the write power more than the read power. There is an average of 46% write power is saved during write '0' and 48% during write '1' operations. The write delay has also been improved about 26% for write '0' and 22% for write '1'

operations compared to 6T SRAM Cell. For read operations, an average of 12% read power and 15% read delay are more compared with 6T cell. Other than power and delay, the HPLP cell also proves that it can work for various V_{DD} ranging from 1.8V to 0.8V and be stable in any worse conditions with temperature ranging from -50°C to 150°C. The proposed HPLP cell is robust for write operations and certainly a better choice with its higher stability and less power consumption for any relevant IOT applications

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