# Amplitude Modulation Index Based Equation For Predicting Total Harmonics Distortion In Seven Level Cascaded H-Bridge Inverter

Douglas T. kureve, Nentawe Y. Goshew, Samuel T. Awuhe

**Abstract**: This research work focuses on developing an amplitude modulation index based equation that can predict the harmonic content in the conventional seven-level cascaded H-bridge multilevel inverter (CHBMLI) at low switching frequency. A logic circuit using phase opposition disposition pulse width modulation (PODPWM) scheme is used for the seven-level CHBMLI. The multilevel inverter (MLI) is simulated for amplitude modulation indices from 0.10 to 0.26.The simulated and calculated results of the harmonic content in the output voltage at amplitude modulation index of 0.20 produce minimum values of 16.61 % and 13.00 % respectively. The harmonic content from the amplitude modulation equation, on average, deviates from the simulated result by 2.74 %. Simulation results are obtained using MATLAB/SIMULINK software.

**Index Terms**: Alternate phase opposition disposition, cascaded H-Bridge inverter, multilevel inverter, phase disposition, phase opposition disposition, pulse width modulation, total harmonic distortion.

## 1 INTRODUCTION

THe use of inverters has become widespread to compensate for energy shortages where there are frequent power outages. Inverters also provide clean sources of energy devoid of pollution which has made it to attract huge attention. However, traditional inverters are limited to low power and voltage applications. This has given MLIs advantage over traditional inverters for high power and voltage applications due to their increased number of levels at the output. As number of levels increases, the harmonics are reduced and output voltage tends to become more pure [1]. MLIs have switches through which the output voltage levels can be controlled. Pulse width modulation (PWM) schemes are usually employed for switching them. The aim of this paper is to develop an equation for predicting the total harmonic content in the output voltage at some given values of amplitude modulation indices from 0.08 to 0.28. This paper designs a PODPWM modulation circuit that uses logic gates to control an open loop single phase seven-level CHBMLI.

## 2 SEVEN-LEVEL CHBMLI

The conventional seven-level CHBMLI has three half bridges which consist of twelve switching regulators. Each half bridge has a separate direct current (DC) voltage with three levels (+Vdc, 0, -Vdc), so the output voltage levels in the MLI are (+3Vdc, +Vdc, +Vdc, 0, -Vdc, -2Vdc, -3Vdc) [2].

The PODPWM based logic circuit involves the sampling of six carrier signals to produce the required seven output voltage level. The carrier signals are compared with modulating signal to produce the desired output. The modulation scheme for cascaded H-bridge (CHB) inverters involves two parameters called frequency modulation ratio or index ($m_f$) and amplitude modulation ratio or index ($m_a$). These modulation indices are derived from the various parameters that contribute to the efficiency of the inverter [3] It can be shown that for n-level CHBMLI, the amplitude modulation index and frequency modulation index [4] are given by (1) and (2):

$$m_a = \frac{A_m}{(n-1)A_c} \quad (1)$$

$$m_f = \frac{f_c}{f_m} \quad (2)$$

where $A_m$ is the amplitude of the modulating signal,$A_c$ is the amplitude of the carrier signal, $f_c$ is the frequency of the carrier signal and $f_m$ is the frequency of the modulating signal. The schematic diagram of the inverter is shown in Fig. 1.


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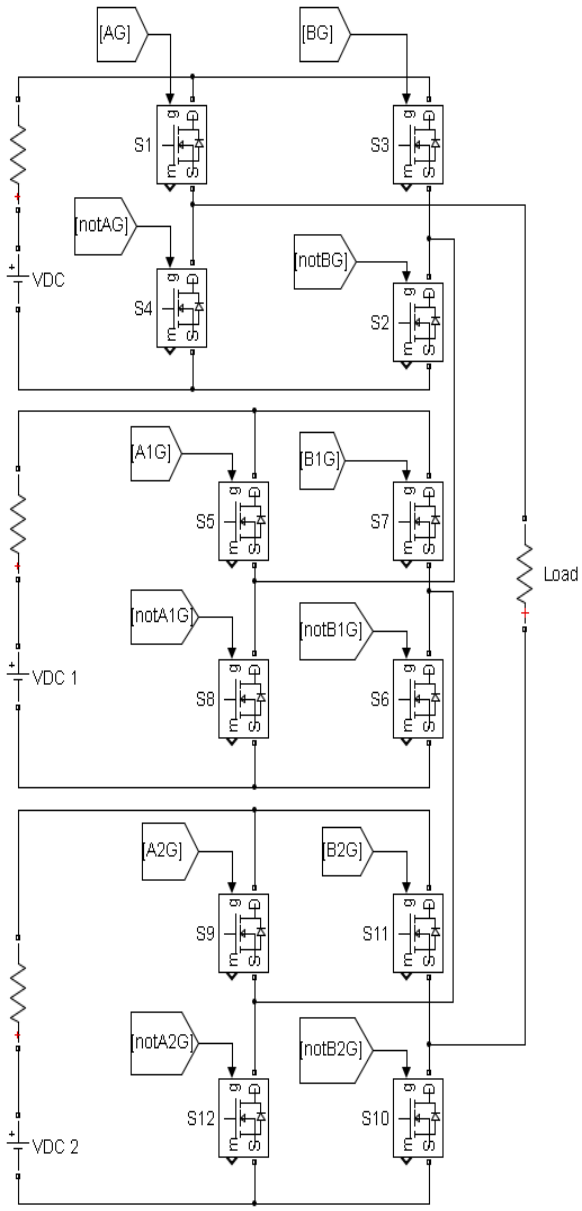


***Fig.1.*** *Seven-level CHB inverter*

## 3 MULTICARRIER PULSE WIDTH MODULATION SCHEME

The carrier modulation methods for MLIs are divided into two categories [5] which are phase-shifted and level-shifted modulation schemes. Both modulation schemes can be applied to the CHB inverters. The level shifted multicarrier modulation method is divided into three [6] namely: phase opposition disposition (POD) method, alternate phase opposition disposition (APOD) method and phase disposition (PD). But this paper focuses on the POD technique.

### 3.1 PODPWM Method

In this scheme, all the carrier waveforms above zero reference are in phase but they are π radians out of phase with the carrier signals below it [7]. The PODPWM scheme is divided equally into two groups according to the positive and negative average levels. The waveform is shown in Fig. 2.

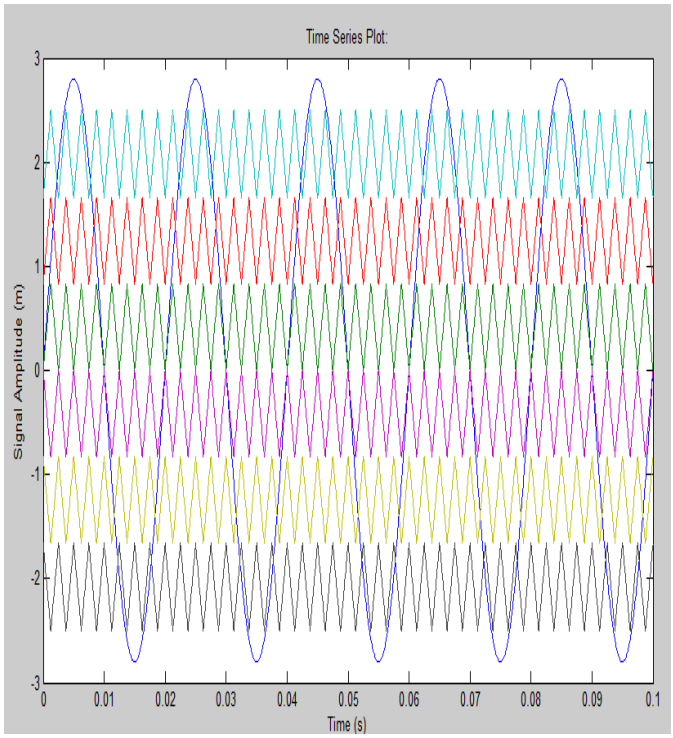


***Fig.2.*** *PODPWM Waveform*

The switching table upon which the PODPWM logic modulation circuit is implemented for the cascaded inverter is given in Table1. The inverter switches are numbered from s1 to s12.

***TABLE1***

*SWITCHING TABLE FOR SEVEN-LEVEL CHB INVERTER*

| S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 | Vdc |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | +3V dc |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | +2V dc |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | +V dc |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 v dc |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -V dc |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | -2V dc |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | -3V dc |

The states of the switches in Table1 are indicated by ones and zeros. Each “1” indicates that the switch is ON and “0” indicates the OFF state of the switch. The vdc is the direct current output voltage.

## 4 SWITCHING LOGIC EQUATIONS

The operation of a seven-level CHB inverter requires six carrier waveforms with a single modulating waveform. At each instant, the carrier signals are compared with the modulating signal to produce pulses for the switches of inverter numbered from $S_1 to S_{12}$ [8] as shown in Fig. 3.

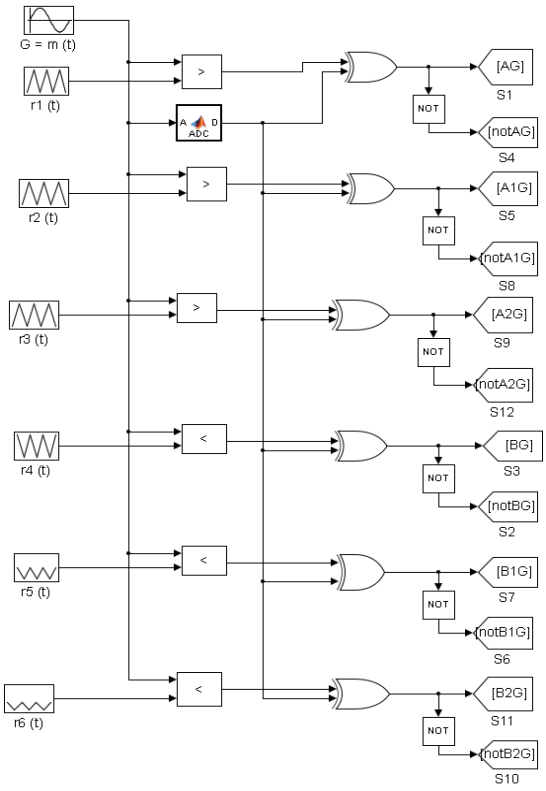


***Fig. 3.*** *PODPWM logic circuit for the CHB inverter*

G = m is the modulating signal and r1, r2, r3, r4, r5, r6 are the carrier signals.

## 5 TOTAL HARMONIC DISTORTION (THD) ANALYSIS

THD is the summation of all harmonic components of the voltage or current waveform compared against the fundamental component of the voltage or current waveform [9]. The formulae for THD components of voltage and current are given in (3) and (4).

$$THD_v = \frac{\sqrt{\sum_{i=2}^{n} V^2}}{V} \quad (3)$$

$$THD_i = \frac{\sqrt{\sum_{i=2}^{n} I^2}}{I} \quad (4)$$

where V and I are the $i^{th}$ voltage and current harmonic values respectively.

## 6 SIMULATION RESULTS

The simulation of the PODPWM logic circuit driven CHBMLI is done using MATLAB/SIMULINK. The FFT tool of Powergui is used to display the frequency spectrum of voltage waveforms. The fundamental component and THD of the output voltages are displayed above the spectrum window. Harmonics are displayed in percent of the fundamental component [10]. The DC source for each half bridge of the CHB inverter is 100 V and an internal resistance of 0.085Ω is considered for the battery. The proposed 8.4kVA seven-level CHB inverter was simulated on a resistive load of 14Ω for amplitude modulation indices from 0.10 to 0.26.

### 6.1 Output Voltage Waveforms at Different Amplitude Modulation Indices

The THD components of output voltage are determined at various amplitude modulation indices ranging from 0.10 to 0.26 at an interval of 0.02. The voltage waveform where the least THD is achieved at modulation index of 0.20 is shown in Fig. 4.

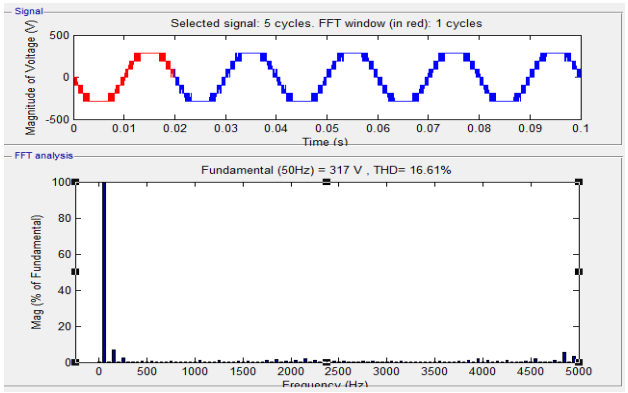


***Fig. 4.*** *Output voltage waveforms and THD spectrum at* $m_a = 0.20$

Simulation is carried out at different modulation indices to display waveforms similar to the waveforms represented in Fig. 4 and the results are tabulated in Table 2.

***Table 2***
*Modulation Index Variation Table for Voltage and THD*

| $m_a$ | Voltage component (V) | THD component (%) |
|---|---|---|
| 0.10 | 175.70 | 34.37 |
| 0.12 | 213.00 | 29.53 |
| 0.14 | 241.40 | 25.65 |
| 0.16 | 275.50 | 22.11 |
| 0.18 | 300.90 | 17.91 |
| 0.20 | 317.00 | 16.61 |
| 0.22 | 326.10 | 17.19 |
| 0.24 | 333.20 | 19.18 |
| 0.26 | 338.70 | 20.01 |

A graph of harmonic content in output voltage against amplitude modulation index is plotted in Fig. 5.

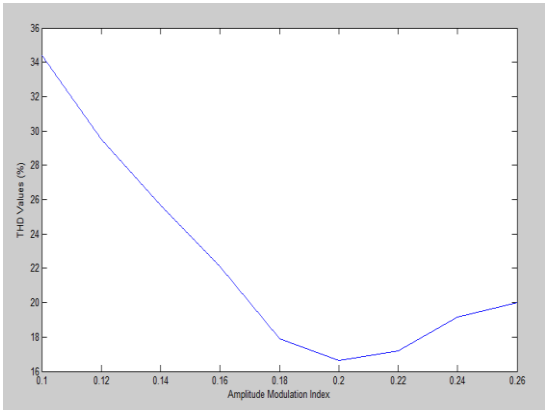


***Fig. 5.*** *Graph of THD against amplitude modulation index*

The equation obtained from the graph of figure 5 is given in (5)

$$y = -1.1e+05x^4 + 8.5e+04x^3 - 2.2e+04x^2 + 2.1e+03x - 31 \quad (5)$$

The calculated values of THD from the equation and the simulated values are tabulated in Table 3.

***TABLE 3***
*TABLE WITH SIMULATED AND CALCULATED THD VALUES*

| Amplitude Modulation Index ($m_a$) | Simulated THD value (%) | THD value from predicted equation (%) | THD deviated value (%) |
|---|---|---|---|
| 0.10 | 34.37 | 33.00 | 1.37 |
| 0.12 | 29.53 | 28.27 | 1.26 |
| 0.14 | 25.65 | 22.78 | 2.87 |
| 0.16 | 22.11 | 17.87 | 4.24 |
| 0.18 | 17.91 | 14.45 | 3.46 |
| 0.20 | 16.61 | 13.00 | 3.61 |
| 0.22 | 17.19 | 13.60 | 3.59 |
| 0.24 | 19.18 | 15.89 | 3.29 |
| 0.26 | 20.01 | 19.08 | 0.93 |

## 7 DISCUSSION OF RESULTS

The voltage waveforms for simulated PODPWM logic circuit driven CHBMLI at modulation index of 0.20 are shown in Fig. 4. Simulation is carried out at different amplitude modulation indices to display waveforms similar to the waveforms represented in Fig. 4 and the results are tabulated in Table 2. A graph of harmonic content in output voltage against amplitude modulation index is plotted in Fig. 5 and equation 5 is obtained for the relationship between the two variables. The calculated values of THD from the equation and the simulated values are tabulated in Table 3.

## 8 CONCLUSION

It can be seen from the simulated and calculated results that the harmonic content in the output voltage at amplitude modulation index of 0.20 attains minimum values of 16.61 % and 13.00 % respectively. The THD values obtained from the equation deviate from the simulated values by 2.74 % on average. The highest and least deviations of 4.24 % and 0.93 % occur at amplitude modulation indices of 0.16 and 0.26 respectively. This paper shows that the harmonic content can be predicted from the modulation indices of 0.08 to 0.28 using the designed equation.

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